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C14–EE–505

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BOARD DIPLOMA EXAMINATION, (C–14)

MARCH/APRIL—2017

DEEE—FIFTH SEMESTER EXAMINATION

DIGITAL ELECTRONICS

Time : 3 hours] [*Total Marks* : 80

PART—A 3×10=30

Instructions : (1) Answer **all** questions.

(2) Each question carries **three** marks.

(3) Answers should be brief and straight to the point and shall not exceed *five* simple sentences.

1. Convert the decimal number 63 into binary, BCD and octal.

2. Subtract 14_{10} from 19_{10} using 2's complement method.

3. List any three IC numbers of two input digital IC logic gates.

4. Define the following characteristics of digital ICs :

(a) Fan-out

(b) Propagation delay

5. Classify the digital logic families.

6. Draw the logic diagram of half-adder using NAND gates only.

7. List any three applications of decoders.

8. Distinguish between synchronous and asynchronous countrs.

9. Briefly explain the race around condition.

10. List any three applications of shift-registers.

PART—B 10×5=50

Instructions : (1) Answer *any* **five** questions.

(2) Each question carries **ten** marks.

(3) Answers should be comprehensive and the criterion for valuation is the content but not the length of the answer.

11. *(a)* Simplify the logic expression $ABC \quad AB\overline{C} \quad A\overline{B}C \quad \overline{A}BC$ using Karnaugh map. 5

(b) State and explain the De Morgan's theorems. 5

12. Draw CMOS NAND gate and explain its operation. 10

13. *(a)* Compare the TTL, CMOS and ECL logic families. 5

(b) Draw the TTL, NAND gate with open-collector. 5

14. *(a)* State the need of tri-state buffer. 2

(b) Draw and explain operation of 3 8 decoder. 8

15. Draw and explain 2'complement parallel adder/subtractor. 10.

16. Draw and explain the asynchronous decade counter. 10

17. *(a)* List any three applications of flip-flops. 3

(b) Draw and explain the operation of clocked *J-K*-flip-flop. 7

18. *(a)* Briefly explain *(i)* memory read operation, *(ii)* access time and *(iii)* memory capacity. 3

(b) Draw and explain the working of 4-bit shift left register. 7

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